FIG. 1
RELATED ART

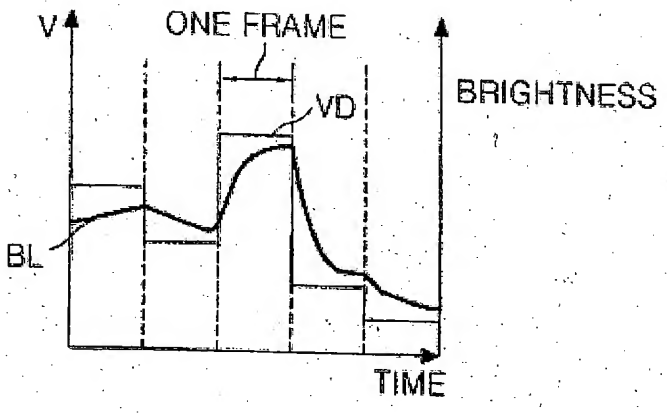


FIG. 2
RELATED ART

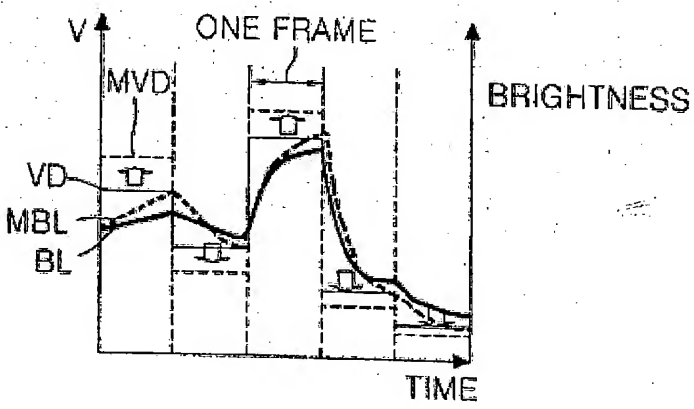


FIG.3
RELATED ART

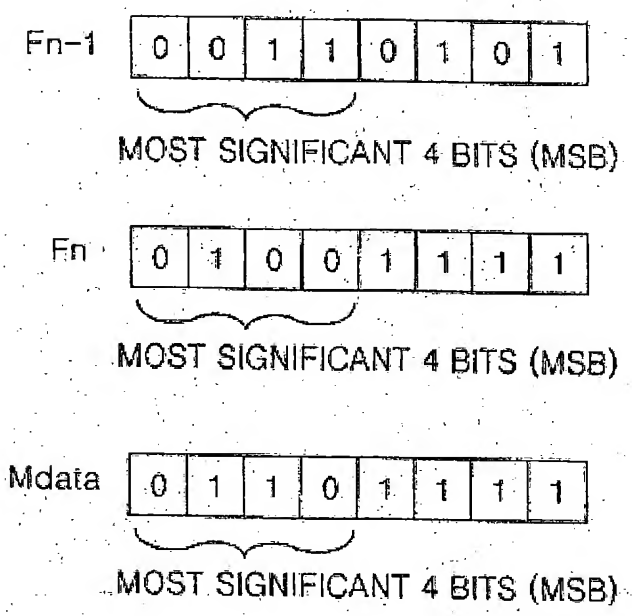


FIG. 4
RELATED ART

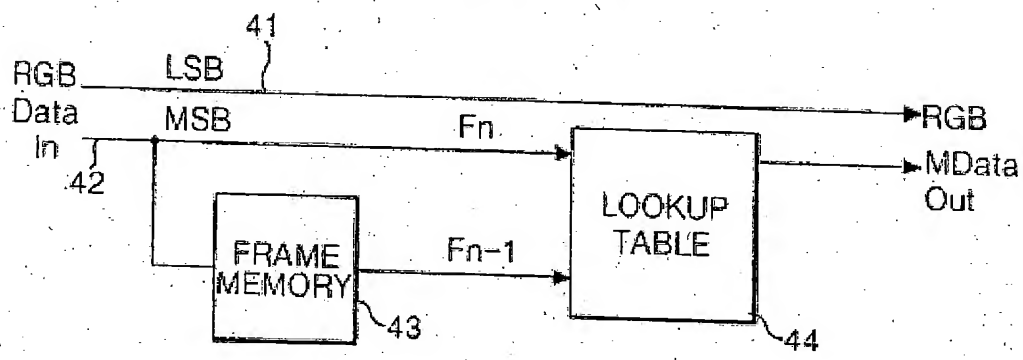


FIG.5

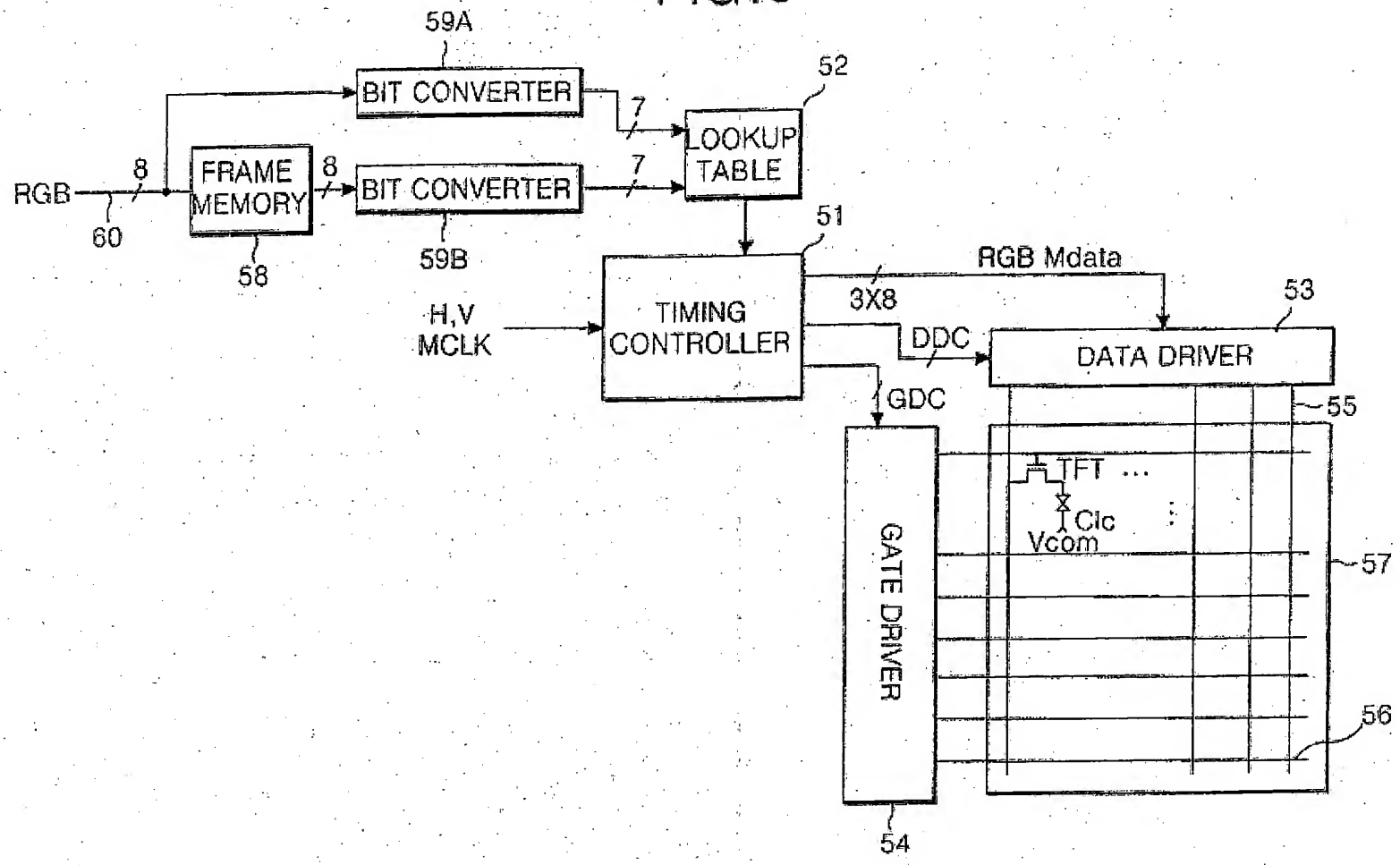

59A
BIT CONVERTER
52
7
LOOKUP TABLE
RGB
8
60
FRAME MEMORY
8
58
BIT CONVERTER
7
59B
51
RGB Mdata
3X8
53
H,V
MCLK
TIMING CONTROLLER
DDC
DATA DRIVER
GDC
55
TFT
Clc
Vcom
57
GATE DRIVER
56
54

FIG.6

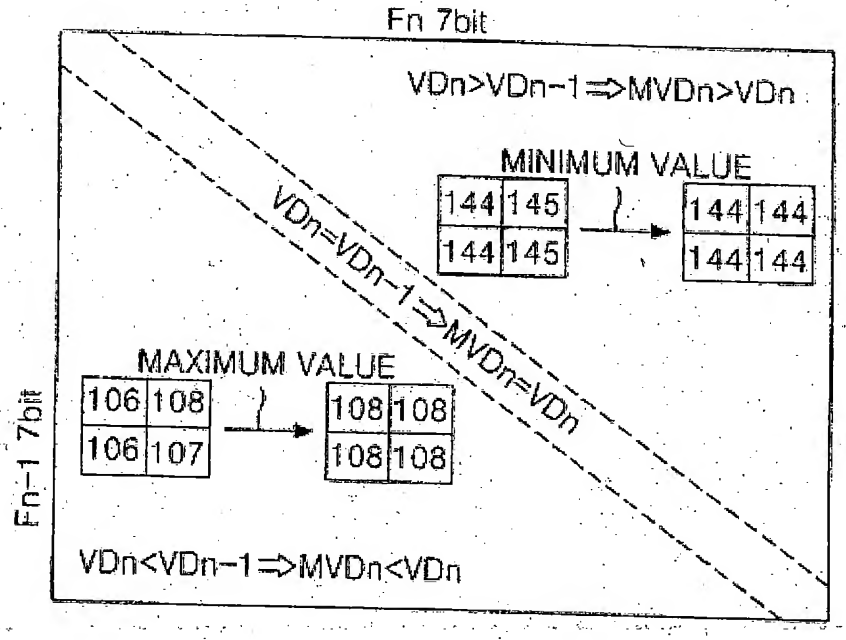

Fn 7bit
VDn>VDn-1⇒MVDn>VDn
MINIMUM VALUE
144 145
144 145
144 144
144 144
VDn=VDn-1⇒MVDn=VDn
MAXIMUM VALUE
106 108
106 107
108 108
108 108
Fn-1 7bit
VDn<VDn-1⇒MVDn<VDn

FIG. 7

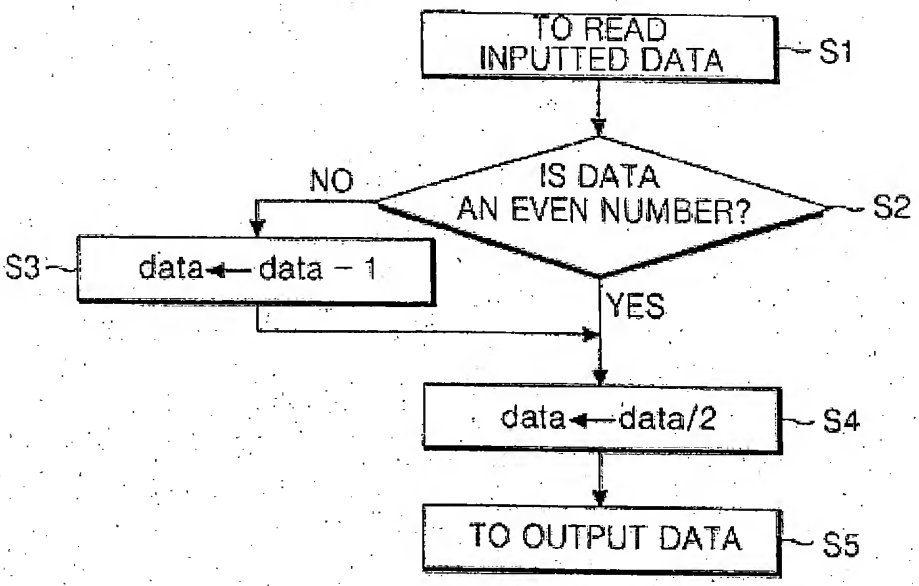
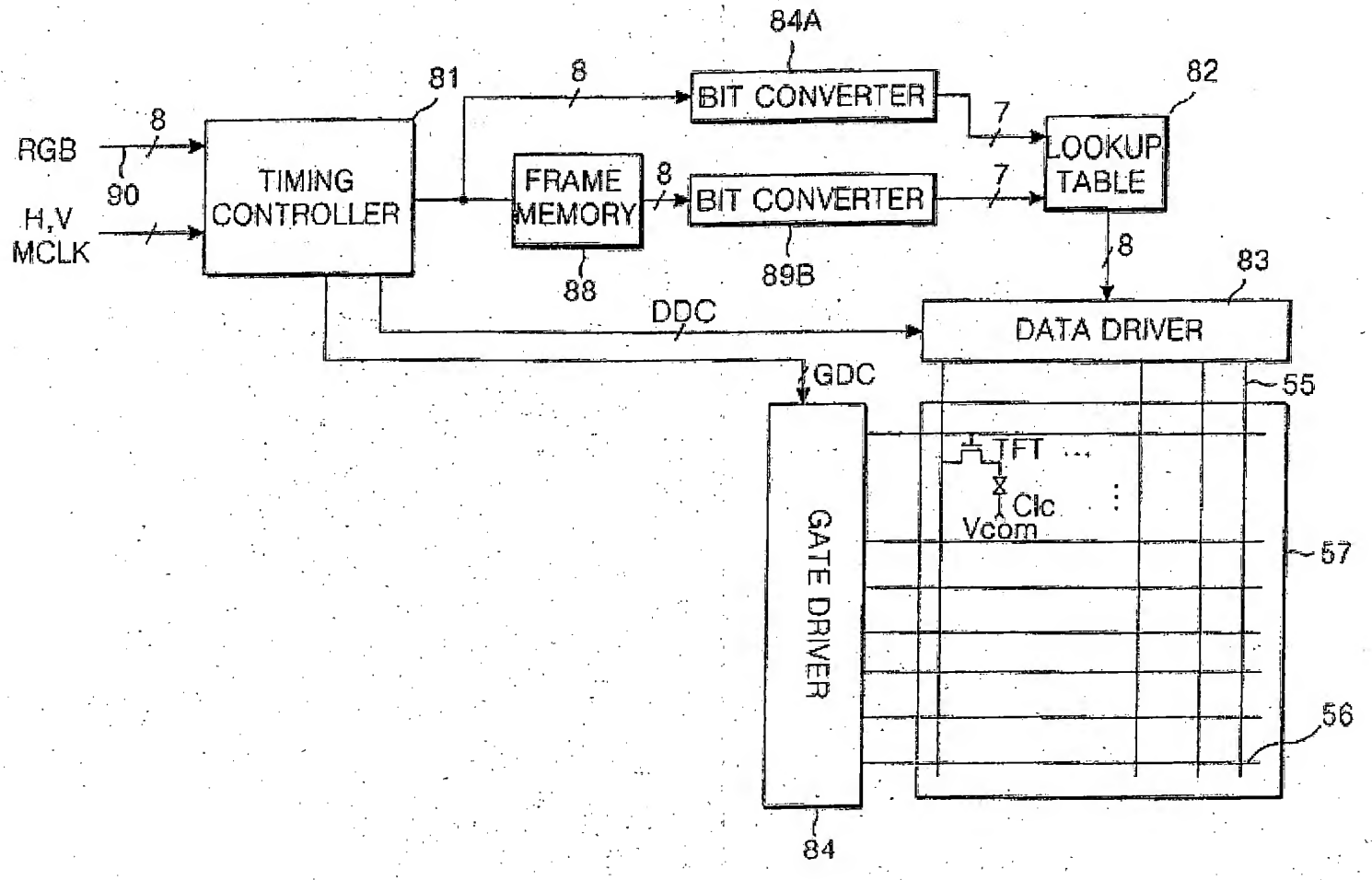

TO READ INPUTTED DATA
S1
IS DATA AN EVEN NUMBER?
S2
NO
YES
S3
data ← data − 1
data ← data/2
S4
TO OUTPUT DATA
S5

FIG.8


84A
81
8
82
BIT CONVERTER
7
LOOKUP TABLE
RGB
8
90
TIMING CONTROLLER
FRAME MEMORY
8
BIT CONVERTER
7
H,V
MCLK
88
89B
8
83
DDC
DATA DRIVER
GDC
55
FT
Clc
Vcom
57
GATE DRIVER
56
84

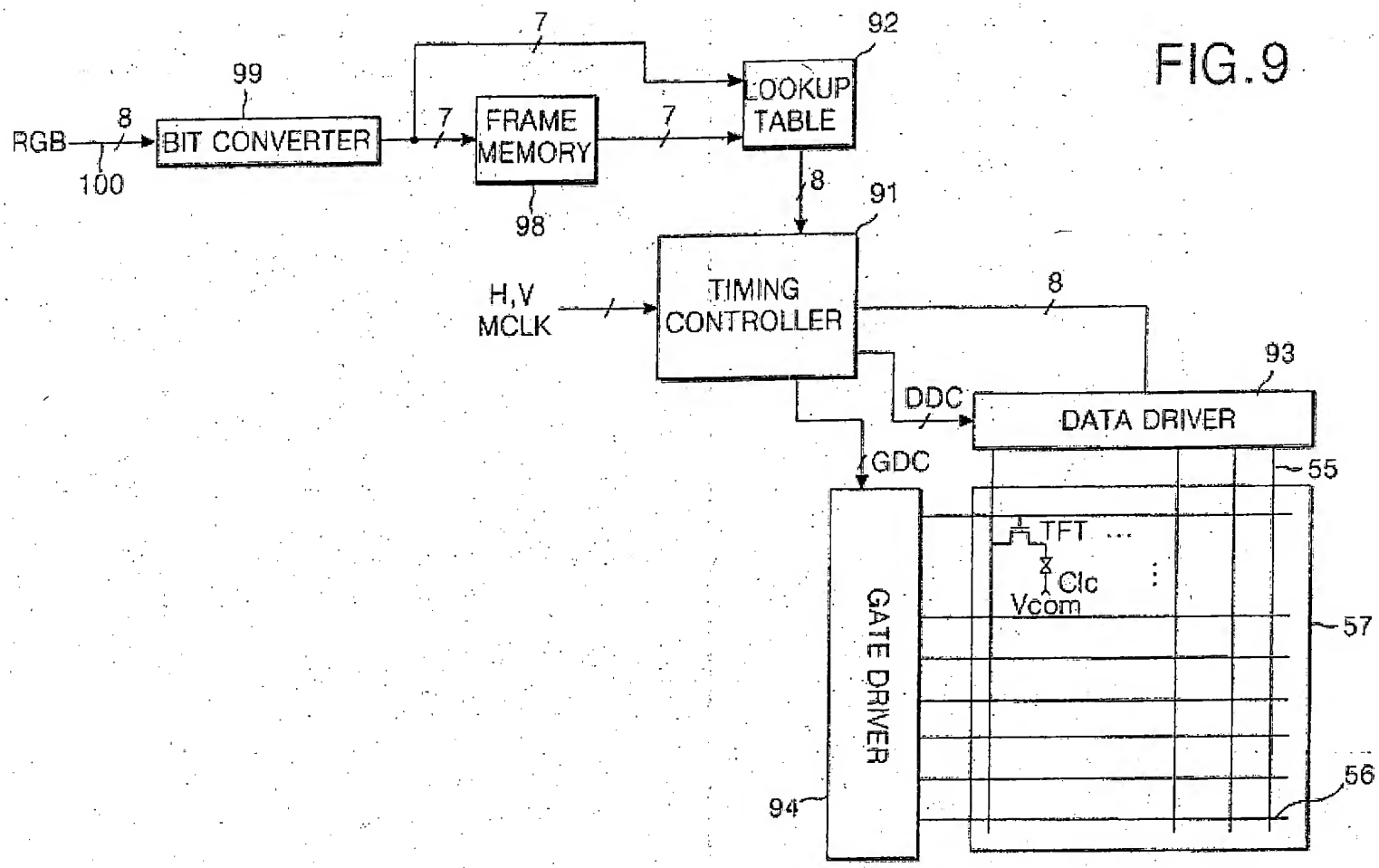
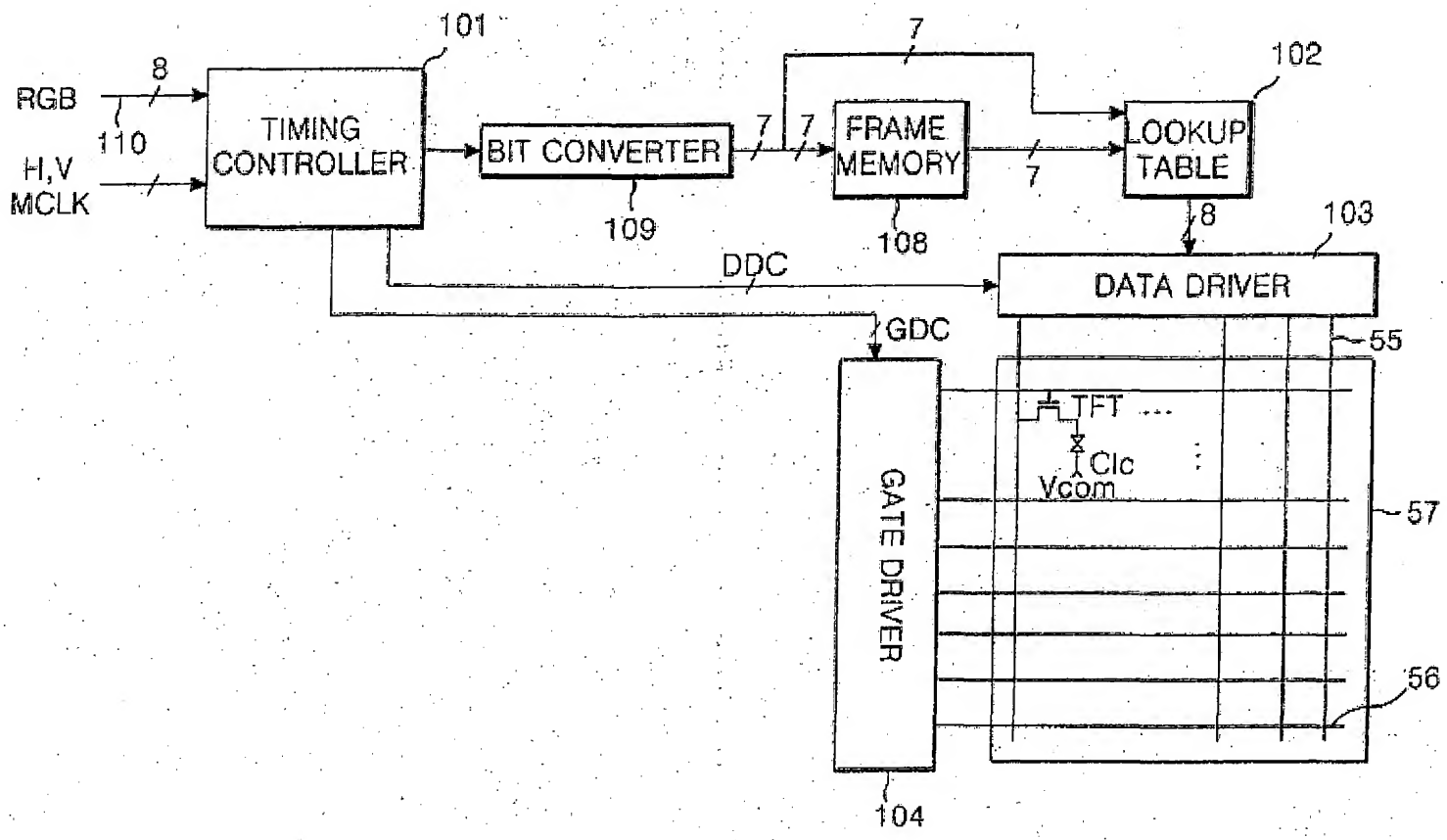

RGB
8
100
99
BIT CONVERTER
7
7
FRAME MEMORY
98
7
92
LOOKUP TABLE
8
91
H,V
MCLK
TIMING CONTROLLER
8
93
DDC
DATA DRIVER
GDC
55
TFT
Clc
Vcom
57
GATE DRIVER
94
56

FIG.9

FIG.10


RGB
H,V
MCLK
8
110
101
TIMING CONTROLLER
BIT CONVERTER
109
7
7
7
FRAME MEMORY
108
7
102
LOOKUP TABLE
8
103
DATA DRIVER
DDC
GDC
55
TFT
Clc
Vcom
57
56
GATE DRIVER
104

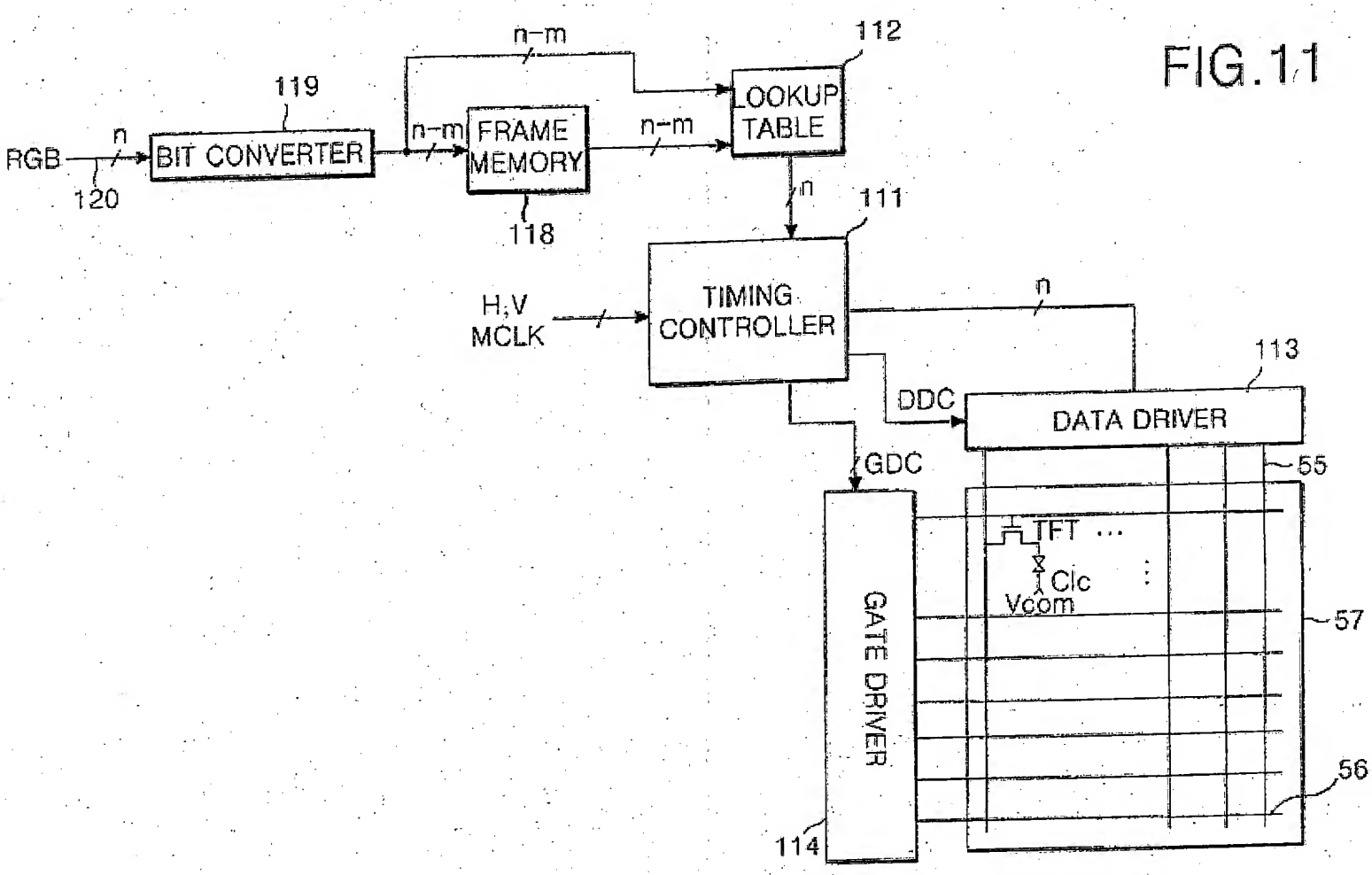

n-m
112
119
LOOKUP TABLE
RGB
n
BIT CONVERTER
n-m
FRAME MEMORY
n-m
120
118
n
111
H,V
MCLK
TIMING CONTROLLER
n
113
DDC
DATA DRIVER
GDC
55
TFT
Clc
Vcom
57
GATE DRIVER
56
114

FIG.11

FIG.12

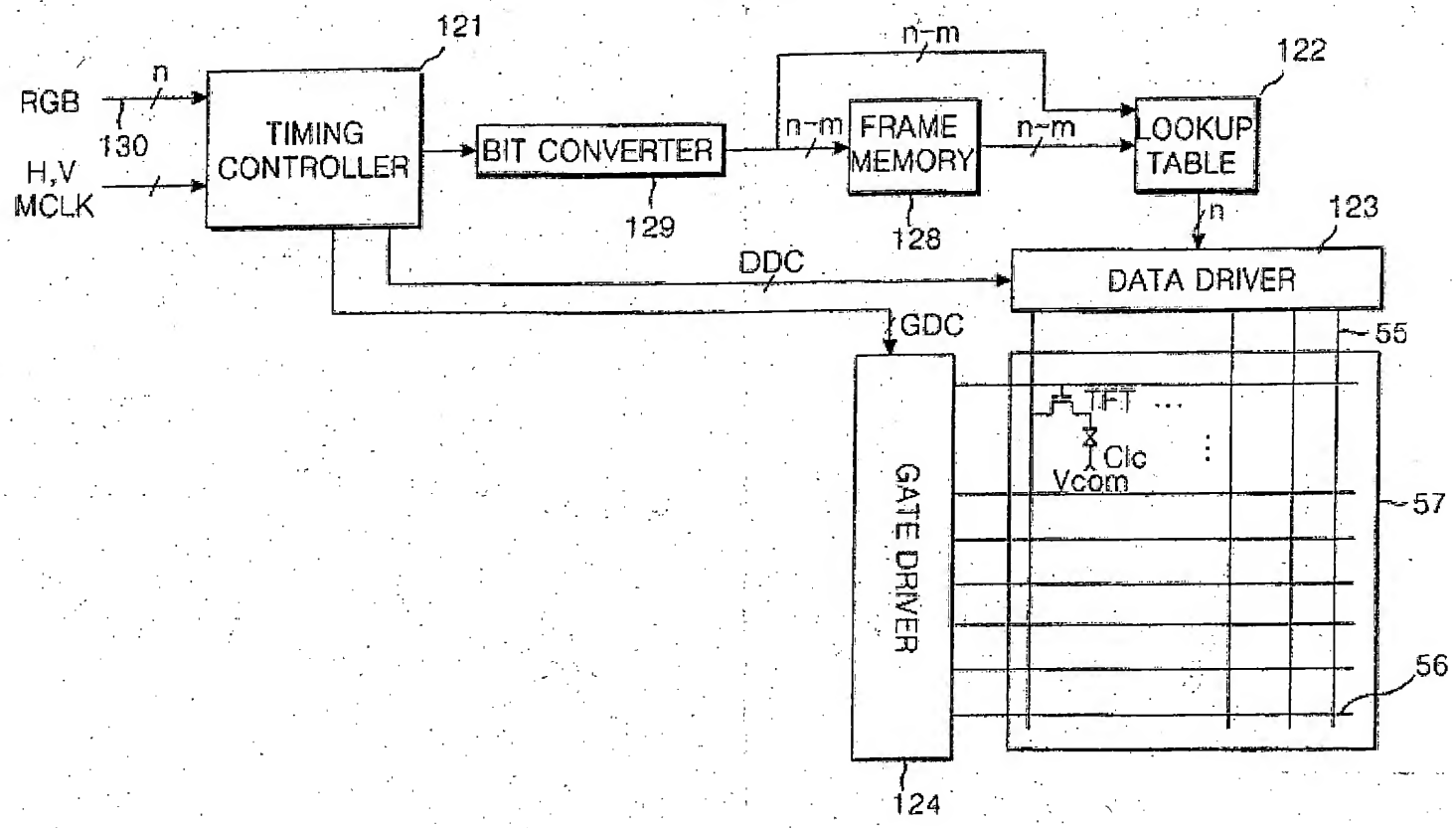

RGB
H,V
MCLK
n
130
TIMING CONTROLLER
121
BIT CONVERTER
129
n-m
FRAME MEMORY
128
n-m
LOOKUP TABLE
122
n
DDC
GDC
DATA DRIVER
123
55
TFT
Clc
Vcom
GATE DRIVER
124
57
56

FIG.13

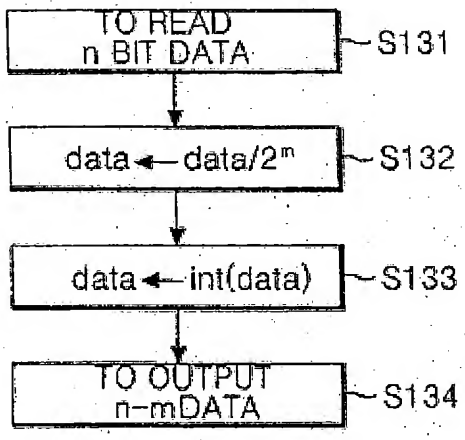

TO READ
n BIT DATA
S131
data ← data/2^n
S132
data ← int(data)
S133
TO OUTPUT
n-mDATA
S134

FIG.14

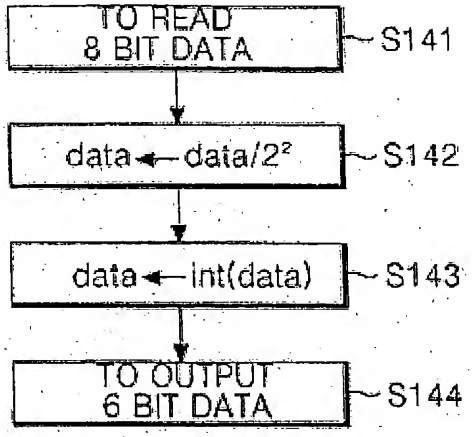

TO READ
8 BIT DATA
S141
data ← data/2²
S142
data ← int(data)
S143
TO OUTPUT
6 BIT DATA
S144

FIG. 15

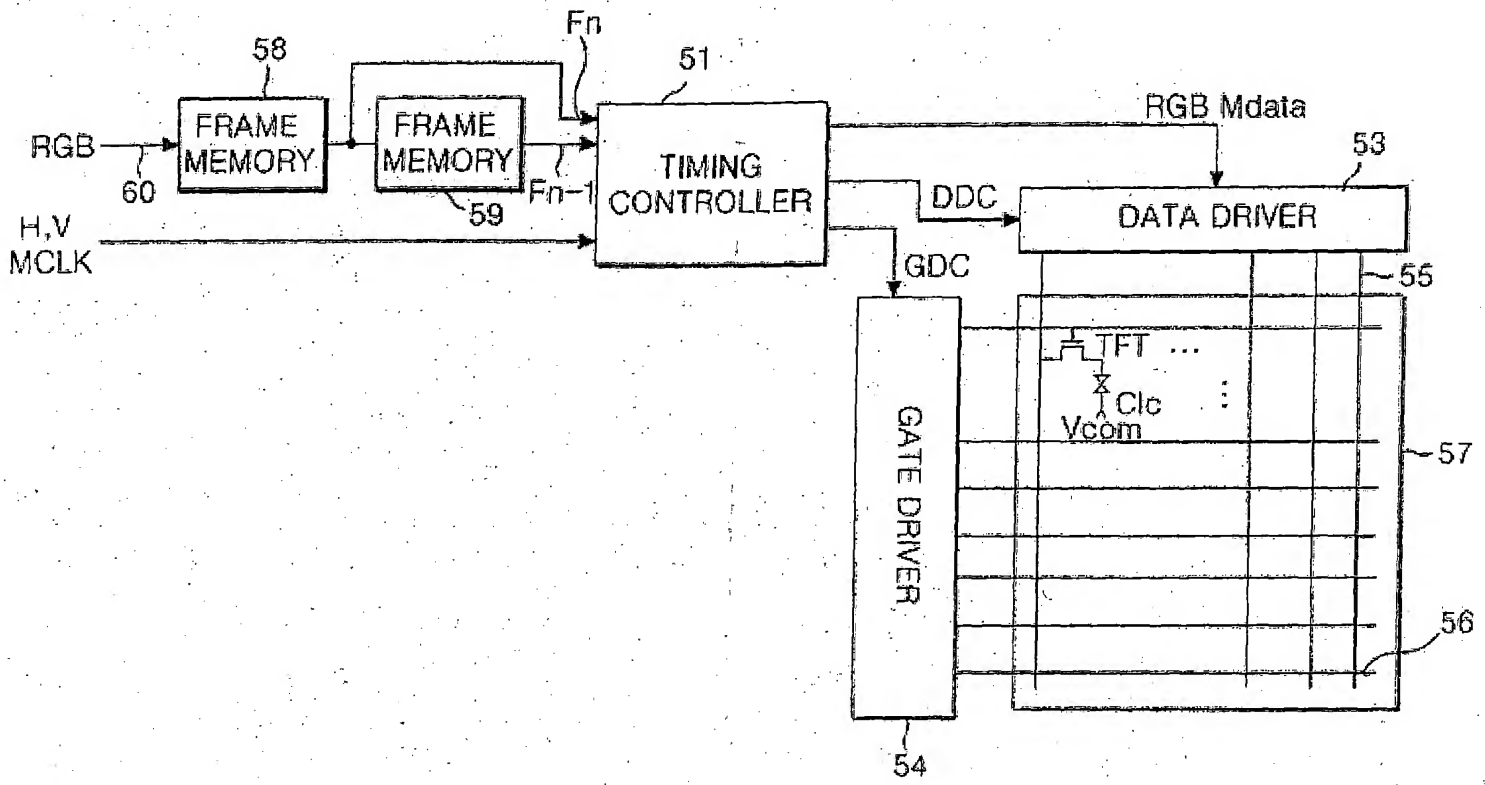

RGB
60
FRAME MEMORY
58
FRAME MEMORY
59
Fn
Fn-1
H,V
MCLK
TIMING CONTROLLER
51
RGB Mdata
53
DDC
DATA DRIVER
GDC
55
TFT
Clc
Vcom
GATE DRIVER
54
57
56

FIG.16

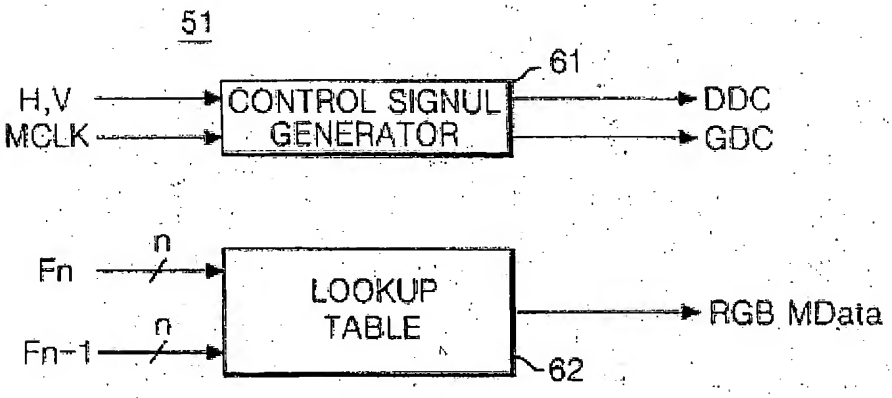

51
61
H,V
MCLK
CONTROL SIGNUL GENERATOR
DDC
GDC
n
Fn
n
Fn-1
LOOKUP TABLE
RGB MData
62

FIG.17

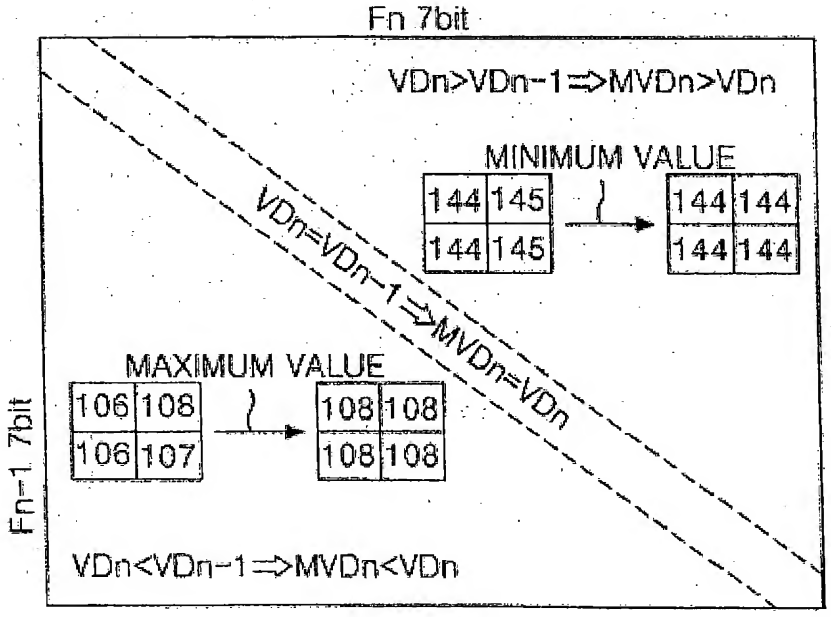

Fn 7bit
Fn-1 7bit
VDn>VDn-1⇒MVDn>VDn
MINIMUM VALUE
144 145
144 145
144 144
144 144
VDn=VDn-1⇒MVDn=VDn
MAXIMUM VALUE
106 108
106 107
108 108
108 108
VDn<VDn-1⇒MVDn<VDn

FIG.18

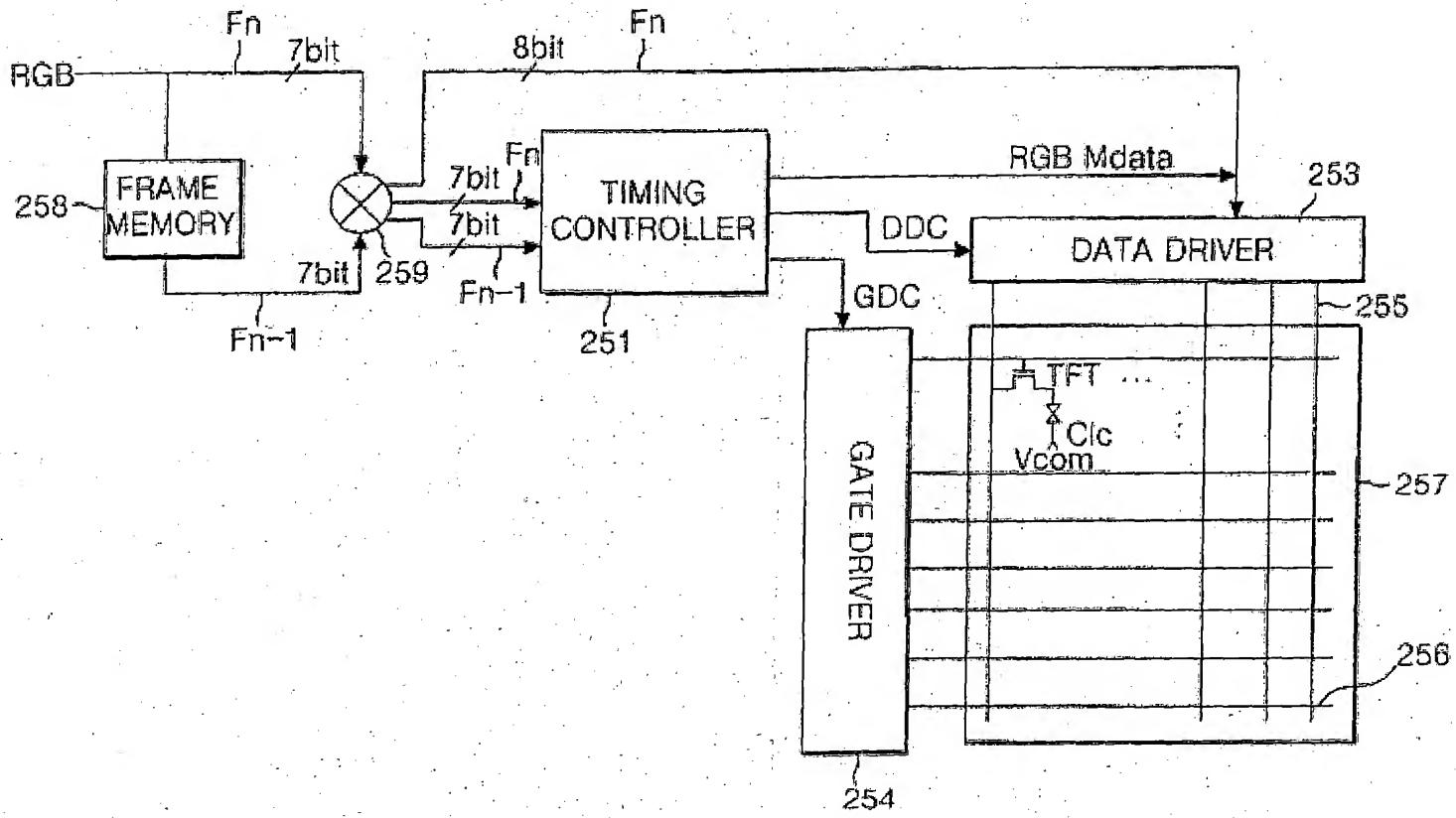

RGB
Fn
7bit
8bit
Fn
258
FRAME MEMORY
7bit
259
7bit
Fn
7bit
Fn-1
Fn-1
TIMING CONTROLLER
251
RGB Mdata
253
DDC
DATA DRIVER
GDC
255
TFT
Clc
Vcom
257
GATE DRIVER
256
254

FIG.19

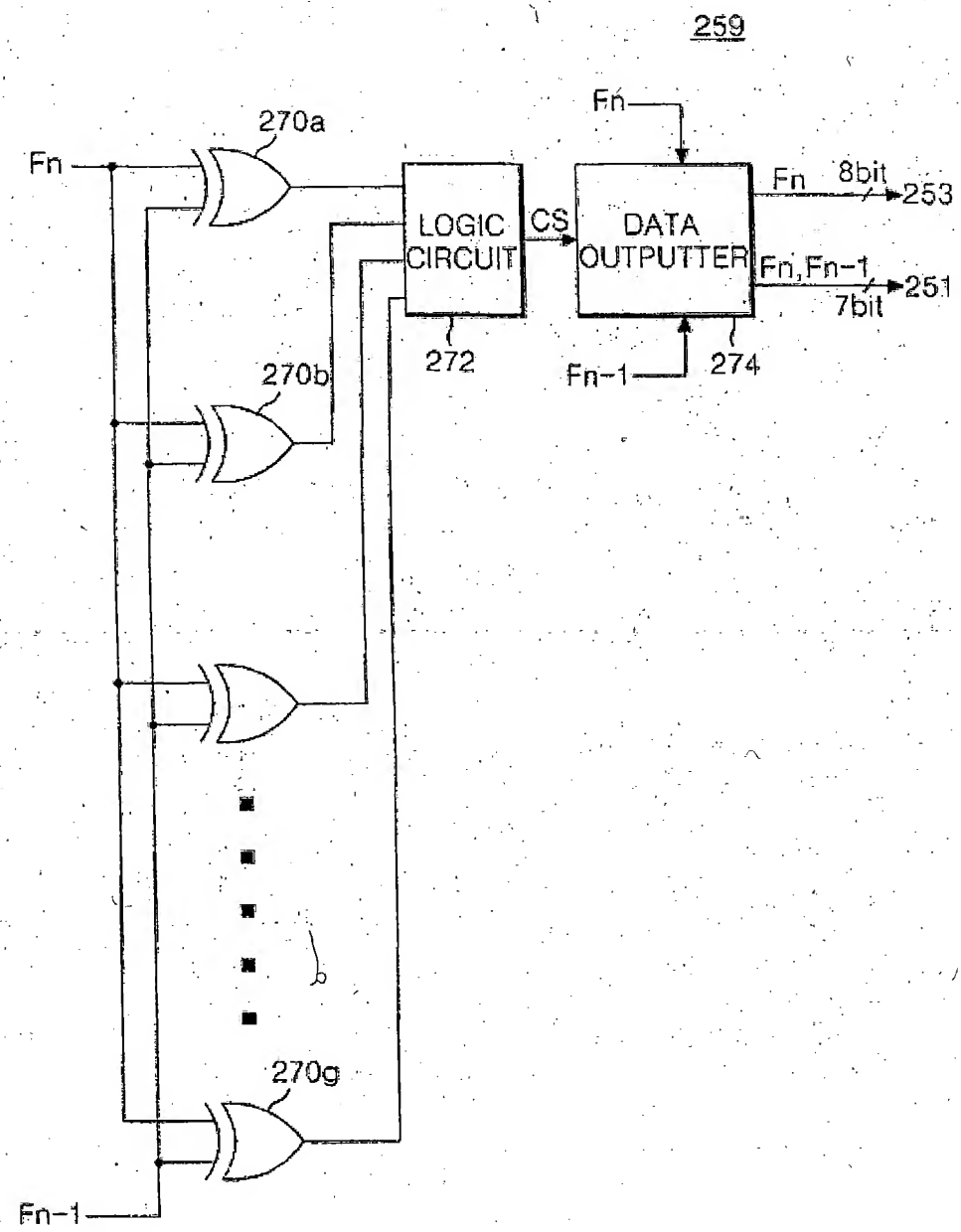
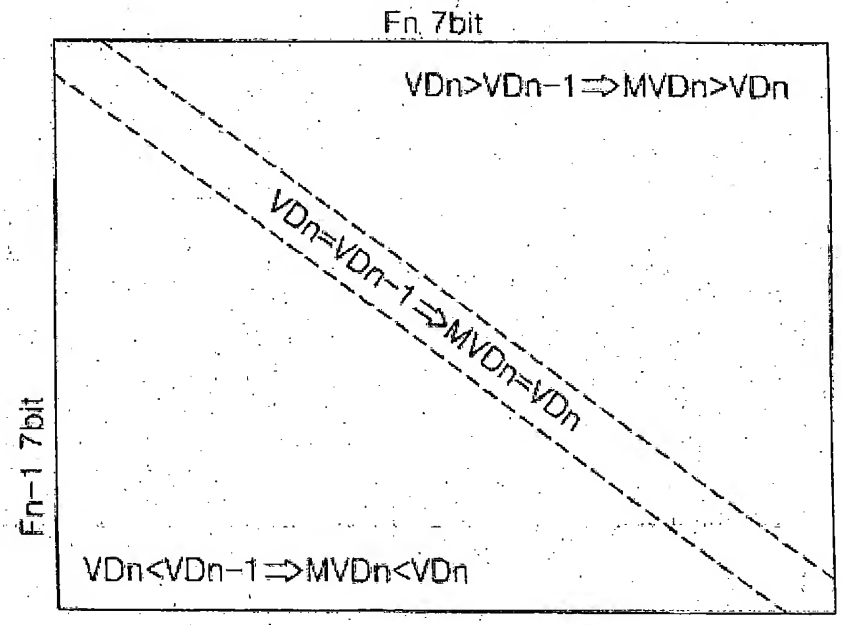

259
Fn
270a
Fn
LOGIC CIRCUIT
CS
DATA OUTPUTTER
Fn 8bit
253
Fn,Fn-1
7bit
251
272
Fn-1
274
270b
270g
Fn-1

FIG.20


Fn 7bit
VDn>VDn-1⇒MVDn>VDn
VDn=VDn-1⇒MVDn=VDn
Fn-1 7bit
VDn<VDn-1⇒MVDn<VDn